AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 10 with the following amended paragraph:

A bandgap voltage reference circuit is based on addition of two voltages having equal and opposite temperature coefficients, TC. The first voltage is a base-emitter voltage of a forward biased bipolar transistor. This voltage has a negative TC of about –2.2mV/°C and is usually denoted as a Complementary to Absolute Temperature, or CTAT, voltage. The second voltage, which is a Proportional to Absolute Temperature, or ~~a~~ PTAT, voltage, is formed by amplifying the voltage difference (ΔV_{be}) of two forward biased base-emitter junctions of bipolar transistors operating at different current densities. More information on bandgap voltage reference circuits including examples of prior art methodologies can be found in, for example, co-pending U.S. application serial no. 10/375,593 of Stefan Marinca as filed on 27th February 2003, the contents of which are incorporated herein by reference.

Please replace the paragraph beginning on page 1, line 22 with the following amended paragraph:

It will be understood that for a pair of bipolar transistors operating at collector current densities in a ratio of 1[[/]]:50 ΔV_{be} is ~~of~~on the order of about 100mV at room temperature. As a CTAT voltage is typically of the order of about 700mV it will be appreciated that the ΔV_{be} needs to be amplified by ~~an order~~a factor of about 5, in order to balance the CTAT voltage. However this amplification of the ΔV_{be} voltage has the effect of ~~including~~introducing offset voltages into the PTAT voltage and as a result the reference voltage precision may be affected. These errors are greater when the circuitry is implemented using CMOS processes as opposed to similar circuits implemented using bipolar techniques. Such difference in performance can be traced to the fact that

in simple CMOS processes only parasitic bipolar transistors are available and amplifiers based on MOS transistors have larger input voltage offsets.

Please replace the paragraph beginning on page 2, line 3 with the following amended paragraph:

Figure 1 is an example of a conventional CMOS implemented bandgap voltage reference. Three pMOS transistors M1, M2 and M3 are provided, each having the same aspect ratio of width/length (W/L). ~~A f~~First and second bipolar transistors Q1 and Q2 are provided, with transistor Q2 having a larger emitter area as compared to Q1. As a result, transistors Q1 and Q2 operate at [[a]]different current densit[[y]]ies (the emitter currents are the same for both). An amplifier A1, which is coupled to both transistors Q1 and Q2 keeps the two input levels at the same value and as a result a voltage, ΔVbe, is developed across a resistor r1. ΔVbe is of the form

$$\Delta V_{be} = (kT/q)(\ln(n)) \qquad (1)$$

where
k is the Boltzmann constant,
q is the charge on the electron,
T is the operating temperature in degrees Kelvin, and
n is the collector current density ratio of the two bipolar transistors.

Please replace the paragraph beginning on page 2, line 20 with the following amended paragraph:

The voltage reference Vref provided by the circuit can be determined as the base-emitter voltage of Q3 plus the voltage drop over r2[[.]]:

$$Vref = V_{be}Q3 + (r2/r1)(\Delta V_{be}) \qquad (2)$$

Please replace the paragraph beginning on page 2, line 25 with the following amended paragraph:

The scale value of r2/r1 is chosen to be about 5, and as a result the amplifier offset voltage is also amplified by ~~about~~ a factor of about 6, as the input offset voltage is ~~gained~~amplified to the output by a factor of 1+r2/r1. It will therefore be understood that for each 1mV input voltage offset, an error of about 6mV is reflected into the bandgap reference. One way to reduce this offset sensitivity is to stack the bipolar transistors. The stacking is however limited by the available headroom- most circuits have to operate from an available 2.6V supply voltage and as a result the number of stacks is typically limited to 2 or 3. Therefore, although it is known to stack transistors at the input to the amplifier so as to generate a multiple value of ΔV_{be}, as this is generated across the resistor at the input to the amplifier there is still an offset contribution that is ~~gained~~amplified by the circuitry.

Please replace the paragraph beginning on page 3, line 4 with the following amended paragraph:

A further source of error in bandgap voltage reference circuits can be traced to resistor mismatch. As will be evident from an examination of the terms in equation ~~two~~(2), any error in the resistor ratio is directly translated into the reference voltage. It would therefore be desirable to ~~minimise~~minimize this source of error.

Please replace the paragraph beginning on page 3, line 9 with the following amended paragraph:

Yet another source of error can be traced to what is commonly called "curvature". This is a second-order error component. In a bipolar transistor, the base-emitter voltage biased at a PTAT collector current can be given by:

$$V_{be}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{be0}\frac{T}{T_0} - (\sigma - 1)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \quad (3)$$

where:

$V_{be}(T)$is the temperature dependence of the base-emitter voltage for the bipolar transistor at operating temperature T,

V_{be0} is the base-emitter voltage for the bipolar transistor at a reference temperature,

V_{G0} is the bandgap voltage or base-emitter voltage at 0°K,

T_0 is the reference temperature, and

σ is the saturation current temperature exponent.

Please replace the paragraph beginning on page 3, line 22 with the following amended paragraph:

The last (i.e., third) term of equation ~~three~~(3) contributes the curvature, and ideally would be ~~minimised~~minimized.

Please replace the paragraph beginning on page 4, line 6 with the following amended paragraph:

An example of an implementation of a bandgap reference circuit that is specifically designed to reduce the number of resistors ~~utilised~~utilized is given in U.S. Patent No. 6,614,209 of Gregoire, Jr. This describes a bandgap reference circuit ~~utilising~~utilizing multiple PTAT sources coupled in series to generate a final PTAT voltage. A current biased base-emitter region of a bipolar transistor is coupled between the final PTAT voltage and an output terminal of the bandgap voltage reference so as to add the base-emitter voltage to the final PTAT voltage, thereby generating a stable voltage reference. Although this approach enables a reduction in the resistor ratio traditionally used in bandgap circuits, it suffers from a number of drawbacks. As the circuit does not provide for curvature correction, it is necessary to generate a large ΔV_{be} (PTAT) in order to balance the base-~~emiter~~emitter voltage (CTAT). Gregoire, Jr. '209 achieves this balancing by using a two-stage

architecture as shown in Figure 5 of the patent. The required PTAT voltage is provided by the combination of an initial PTAT source, referenced as block 510, and a terminal PTAT source, referenced as block 530, both including amplifiers. Due to the configuration of the circuitry, the second amplifier requires a high headroom environment to operate effectively as its two inputs have a common voltage which is about $3\Delta V_{be}$ (approximately 330mV at room temperature) compared to that of the first amplifier. This limits the applications where this bandgap voltage reference can be ~~utilised~~utilized. Secondly, the requirement for two amplifiers increases the area required and the power supply needed on a die for implementation of such a circuit. Furthermore, as there is no curvature correction provided to the reference, the precision of the reference voltage provided is limited. Additionally, as two amplifiers are used the contribution to offset and noise is increased.

Please replace the paragraph beginning on page 5, line 30 with the following amended paragraph:

_____In accordance with an ~~embodiment~~aspect of the invention, a bandgap voltage reference circuit is provided including an amplifier having first and second input nodes, and providing a reference voltage at an output thereof ~~is provided~~. The circuit additionally includes at least two pairs of transistors, each pair having a first transistor adapted to operate at a different current density to that of the second transistor, such that, in use, a difference in base-emitter voltages, ΔV_{be}, between the two transistors of each pairing is generated. The pairs are arranged such that those transistors having a first current density are provided in a chain coupled to the first input node and those transistors having the second current density are provided in a chain coupled to the second input node, the combination of the ΔV_{be} provided by each pairing contributing to an enhanced ΔV_{be} at the output of the amplifier, the enhanced ΔV_{be} being generated across a resistor provided at the output of the amplifier.

Please replace the paragraph beginning on page 6, line 10 with the following amended paragraph:

Desirably, three pairs of transistors are provided, each of the pairs contributing a ΔV_{be} component, such that the enhanced ΔV_{be} voltage generated across the resistor at the output of the amplifier is equivalent to $3\Delta V_{be}$.

Please replace the paragraph beginning on page 6 line 13 with the following amended paragraph:

In order to ~~maximise~~maximize the effect of the contribution of the $3\Delta V_{be}$ voltage, the circuit is preferably further adapted to generate a curvature correction voltage. This curvature correction voltage may be provided by driving each of the three transistors operating at the first current density with a Proportional to Absolute Temperature (PTAT) current and the other three transistors with a constant current, the sum of the curvature correction voltage and the $3\Delta V_{be}$ voltage being both applied across the resistor on the output of the amplifier, thereby correcting for curvature associated with the bandgap circuit.

Please replace the paragraph beginning on page 7 line 4 with the following amended paragraph:

In certain embodiments, the ~~third pair of~~ transistors of the third pair are both driven with a PTAT current. Such a PTAT current may be generated externally to the circuit.

Please replace the paragraph beginning on page 7 line 23 with the following amended paragraph:

The invention also provides a bandgap voltage reference circuit adapted to provide at an output thereof a reference voltage, the reference voltage being provided by the combination of generated CTAT and PTAT voltages, the CTAT voltage being provided by a base-emitter voltage of a forward-biased transistor and the PTAT voltage being provided by multiple ΔV_{be} voltages, each ΔV_{be} voltage being generated by a pair of bipolar transistors, each of which operates ~~operating~~ at a

different current ~~densities~~density from the other, the PTAT voltage being solely defined by a current applied across a single resistor provided at an output of an amplifier.

Please replace the paragraph beginning on page 7 line 31 with the following amended paragraph:

A further ~~embodiment~~aspect of the invention provides a bandgap voltage reference circuit having an amplifier with a first and second input node and providing at an output thereof a reference voltage, each input node being coupled to a chain of at least two transistors, the transistors being arranged such that the emitter of a first transistor is coupled to the base of a second transistor, the emitter of the second transistor being coupled to the input of the amplifier and the collectors of each transistor being coupled to a reference potential and wherein those transistors in a first chain are adapted to operate at a first current density and those transistors in a second chain are adapted to operate at a second different current density, such that a difference in base emitter voltages between transistors in the first and second chain is provided, the difference being equivalent to a multiple ΔV_{be} voltage and being generated by the current provided across a sole load resistor coupled to the output of the amplifier.

Please replace the paragraph beginning on page 8 line 11 with the following amended paragraph:

Yet a further ~~embodiment~~aspect of the invention provides a temperature reference circuit including an amplifier having at its non-inverting input node at least one bipolar transistor operable at a first current density and in a feedback loop between the output of the amplifier and its inverting input node, at least one bipolar transistor operable at a second current density lower then that of the transistor coupled to the non-inverting input, such that due to the difference in current ~~density~~densities of the transistors coupled to each of the two inputs, a ΔV_{be} voltage is reflected at the output of the amplifier and wherein the transistors coupled to each of the input nodes of the amplifier are driven with PTAT currents such that the ΔV_{be} voltage developed is temperature

sensitive, thereby providing a voltage reference circuit adapted to provide a measurement of temperature.

Please replace the paragraph beginning on page 8 line 22 with the following amended paragraph:

These and other features of the invention will be better understood with reference to the following drawings which are of exemplary embodiments ~~of~~for practicing the invention and are not intended to be construed as limiting in any manner. As will be appreciated by those skilled in the art, modifications and adaptations can be made to the exemplary embodiments described below without departing from the spirit and scope of the invention.

Please replace the paragraph beginning on page 9 line 16 with the following amended paragraph:

The circuit includes an amplifier A1[[,]] which, in accordance with standard techniques, is adapted to keep its two inputs (an inverting and a non-inverting input) at substantially the same level. The operation of an amplifier will be well known to those skilled in the art and for the sake of convenience will not be explained herein. A first transistor Q1, second transistor Q2 and third transistor Q3 ~~transistor~~ are coupled to the non-inverting input of the amplifier and a corresponding set of three transistors Q4, Q5 and Q6 are coupled to the inverting input. Each of these sets of three transistors may be considered as forming a chain of transistors coupled to their respective input nodes. The emitter areas of transistors Q4, Q5 and Q6 are each "n" times that of transistors Q1, Q2 and Q3.

Please replace the paragraph beginning on page 9 line 26 with the following amended paragraph:

Transistors Q1, Q2 and Q3 are arranged such that the emitter of transistor Q1 is coupled to the base of transistor Q2, the emitter of transistor Q2 to the base of transistor Q3 and the emitter of

transistor Q3 to the non-inverting input of the amplifier. Similarly, the base of transistor Q4 is coupled to the emitter of transistor Q5, the base of transistor Q5 to the emitter of transistor Q6 and the emitter of Q4 to the inverting input of the amplifier A1. The collectors of each of the transistors are tied to ground. As such when the bipolar transistors are biased with appropriate currents, a difference in base-emitter voltage is developed from the bipolar stack operating at high current density (Q1, Q2, Q3) to the bipolar stack operating at low current density (Q4,Q5, Q6). Each of the pairings contribute a ΔV_{be}, and when combined a 3 ΔV_{be} difference is provided.

Please replace the paragraph beginning on page 10 line 3 with the following amended paragraph:

At the output of the amplifier, a first nMOS transistor M1 is provided. The gate of the device M1 is coupled to the output of the amplifier. The drain of M1 is coupled to a diode-connected pMOS transistor M5. The reference voltage, Vref, of the circuit, is provided at a node between the source of M1 and the emitter of another transistor Q7. The base of transistor Q7 is coupled to the drain of a further pMOS transistor M6, and across a resistor r1 to ground. The gates of devices M6 and M5 are commonly coupled and are further coupled to the gates of three further pMOS transistors M2, M3 and M4, the sources of which are coupled to a supply voltage and the drains of which are coupled to the emitters of transistors Q1, Q2 and Q3, thereby providing currents I3, I4 and I5 respectively. Constant currents I6, I7 and I8 are provided at the emitters [[or]]of transistors Q4, Q5 and Q6 respectively.

Please replace the paragraph beginning on page 10 line 14 with the following amended paragraph:

Due to the respective differences between the emitter areas of transistors Q1/Q4, Q2/Q5 and Q3/Q6, a difference of ~~three~~ $3\Delta V_{be}$ is reflected across r1. It will be appreciated that the presence of this sole resistor coupled at the output of the amplifier is sufficient to generate the desired ~~three~~ $3\Delta V_{be}$. As a result, the currents I1 and I2, which are mirrored by M5 and M6, are PTAT currents. Similarly the currents I3, I4 and I5, which are forced into the transistors Q1, Q2 and Q3, are also

PTAT currents. As mentioned above, the currents I6, I7 and I8 forced into the bipolar transistors Q4, Q5 and Q6, which are operating at a lower current density than transistors Q1, Q2 or Q3 are constant currents. For each respective pair of transistors, a negative curvature voltage Vcurv is developed of the type:

$$V_{curv}=(kT/q)(\ln(T/T_o)) \qquad (4)$$

Please replace the paragraph beginning on page 10 line 27 with the following amended paragraph:

The PTAT voltage (i.e., $3\Delta V_{be}$) and the sum of the three combined curvature voltages are both applied across r1. As transistor Q7 is also biased at PTAT, the reference voltage will be equal to V_{G0} with the curvature removed.

Please replace the paragraph beginning on page 11 line 3 with the following amended paragraph:

It will also be understood that the amplifier's offset voltage is only reflected across resistor r1, and as r1 is on the output of the amplifier, that this offset voltage is not gained or amplified by the amplifier.

Please replace the paragraph beginning on page 11 line 6 with the following amended paragraph:

Figure 3 shows an alternative embodiment of the technique of the present invention. In this embodiment, a two-stage amplifier is provided and the technique of Figure 2 is implemented using an unbalanced pair of lateral bipolar transistors that provide the first stage of the amplifier. This first stage includes a first transistor Q3 which is provided as a unity emitter area lateral PNP type transistor and a second transistor Q4 of the same type but with an emitter area scaled "n" times that

of Q3. Transistors Q3 and Q4 are both biased with a PTAT current, I8, which is provided typically from an externally generated current source. The load transistors MN1 and MN2 are adapted to ~~equalise~~equalize the currents passing through transistors Q3 and Q4. As a result, a first ΔV_{be} is developed into the amplifier's first stage.

Please replace the paragraph beginning on page 11 line 16 with the following amended paragraph:

The base node of transistor Q3 is equivalent to the non-inverting input of the amplifier shown in Figure 2 and two transistors Q1 and Q2 are stacked there. The emitter of transistor Q2 is coupled to the base of transistor Q3 and the emitter of transistor Q1 to the base of transistor Q2. The collectors of each of transistors Q1 and Q2 are tied to ground.

Please replace the paragraph beginning on page 11 line 20 with the following amended paragraph:

Similarly, the base node of transistor Q4 is equivalent to the inverting input of the amplifier shown in Figure 2 and two transistors Q5 and Q6 are stacked there. The emitter of transistor Q5 is coupled to the base of transistor Q4 and the emitter of transistor Q6 to the base of transistor Q5. The collectors of each of transistors Q5 and Q6 are tied to ground. The emitter areas of each of transistors Q5 and Q6 ~~are~~is scaled "n" times that of transistors Q1 and Q2.

Please replace the paragraph beginning on page 11 line 25 with the following amended paragraph:

The second stage of the "amplifier" of Figure 3 is provided by an nMOS transistor MN3 which is driven by a current source I5. The drain of transistor MN3 is also coupled to the gate of transistor M1. The source of transistor M1 is coupled to the emitter of the PNP transistor Q7, and this common node provides the output node Vref for the circuit. The base of transistor Q7 is coupled via resistor[[,]] r1[[,]] to ground and also to the drain of pMOS transistor M6. The gate of

transistor M6 is coupled to the gate of a further pMOS transistor M5 which is provided in a diode-connected configuration, thereby providing the master component of a current mirror. It will be appreciated that although Figure 3 shows transistor M5 configured as the master component that alternative arrangements could suitably configure transistor M6 as the master, with transistor M5 as a slave device. However, as illustrated in Figure 3, the drain of transistor M5 is coupled to the drain of transistor M1, the mirror provided by the combination of transistors M5 and M6 is also coupled to transistors M2 and M3 which are in turn coupled to the emitters of transistors Q2 and Q1 respectively. As such, the PTAT current generated through resistor r1[[,]] and current I1[[,]] is mirrored as currents I2, I3 and I4 thereby driving each of components transistors Q1, Q2, Q3/Q4 and M1 with a PTAT current, whereas components transistors Q5 and Q6 are coupled to an externally provided current source, which desirably provides a predominately CTAT current. As was detailed above, the first ΔV_{be} is developed across transistors Q3 and Q4 and the other two ΔV_{be}'s are developed from transistors Q1 and Q2 to transistors Q5 and Q6.

Please replace the paragraph beginning on page 12 line 11with the following amended paragraph:

The $3V_{be}(1)$ developed across transistors Q1, Q2, and Q3 and the $3V_{be}(n)$ developed across transistors Q4, Q5 and Q6 are combined, and in a similar fashion to that described with reference to Figure 2, the output voltage is provided with the curvature component removed. One difference in this implementation from that of Figure 2 is that both transistors Q3 and Q4 are biased with the same, preferably PTAT, current I8, whereas in the implementation of Figure 2, one of the transistors forming the third pair is driven with a constant current and the other with a PTAT current. As a result of driving both transistors of the third pair with a current of the same type, the curvature effect is not entirely removed. The effect of the curvature may be ~~minimised~~minimized by driving transistors Q5 and Q6 with a predominantly CTAT current. The driving of transistors Q5 and Q6 with scaled values of PTAT and CTAT current effects a combined output with the curvature inherent to bandgap voltage circuits removed.

Please replace the paragraph beginning on page 13 line 9 with the following amended paragraph:

Transistors Q1 and Q2 are provided in a stack arrangement and are both provided in a diode-connected configuration. Similarly, transistors Q5 and Q6 are provided in a diode-connected configuration with the base of each coupled directly to ~~their~~its respective collector, the base of transistor Q6 also being coupled to the emitter of transistor Q5. A current I7, which is a constant current source desirably provided as a predominant CTAT current and externally generated, is coupled to this pair of transistors. The first stage of the amplifier is provided by the transistors Q3/Q4/Q8/Q9 with the common emitter of transistors Q3 and Q4 being coupled to an externally generated PTAT current, I8. The collectors of transistors Q3 and Q4 are coupled respectively to the collectors of transistors Q8 and Q9, transistor Q8 being provided in a diode-connected configuration. The collector of transistor Q9 is also coupled to the base of a further transistor, Q10, which provides the second stage of the amplifier. Transistor Q10 is also coupled to an externally provided predominately PTAT current, I5. In a similar fashion to the MOS transistors M1, M5 and M6, the bipolar implementation of Figure 4 provides a bipolar transistor provided as a voltage follower, transistor Q7, whose emitter is coupled to a first transistor[[,]] Q11[[,]] of a current mirror such that the current I2 generated across r1 is mirrored as current I4 by transistor Q13 to drive transistors Q2 and Q1. The transistor Q12 is provided as a master mirror and provides a current I2 coupled to the collector of transistor Q7. The reference voltage of the circuit is provided at a node between transistor Q10 and the base of transistor Q7, and as such is directly tapped from the second stage of the amplifier. It will be appreciated that this configuration has a very low offset sensitivity and sensitivity is reduced as the number (n) of pnp bipolar transistors Q4 is increased.

Please replace the paragraph beginning on page 14 line 14 with the following amended paragraph:

The circuit of the present invention uses three pairs of transistors to generate a ΔV_{be} contribution >120mV for each pair. It will be appreciated that if the reference is corrected for curvature the nominal bandgap voltage is about 1.15V. If the reference is not compensated for the

curvature, the nominal voltage is about 1.25V. For the case of the corrected reference, a 1.15V voltage at room temperature is based on a contribution of about 700mV base-emitter voltage (CTAT) and the difference being provided as a PTAT component. This difference is the required PTAT voltage which is 1.15V-0.7V=0.45V. As a result, the required ΔV_{be} voltage for a pair of bipolar transistors operating at different current ~~density~~densities is about 450mV/3=150mV. As ΔV_{be} is generated from an ln(n) component (see equation 1), it is not a simple exercise to get the value >>120mV by simply scaling the ratios of the transistors operating at different current densities. Each of the transistor pairs requires about 0.8V and in most applications the minimum supply voltage is about 2.6V, thereby defining a maximum number of transistors at 3 pairs. To use only $3\Delta V_{be}$ and to have the output voltage at a level where the $3\Delta V_{be}$ has an effect, it is necessary to combine this generation of the $3\Delta V_{be}$ with a curvature correction mechanism. If curvature correction ~~was~~were not provided, then the output voltage would be about 1.25V (the bandgap of silicon) with a bow contribution of about 2.5mV in the normal operating region. By applying curvature correction, the output voltage is provided without such a bow contribution and as such the contribution provided by the 3 ΔV_{be} is more significant. It will be understood that in order to implement such a bandgap voltage reference circuit in a single stage environment, i.e., only having one amplifier, that it is necessary to apply some curvature correction or the voltage generated by the stacks of transistors will not be sufficient to compensate.

Please replace the paragraph beginning on page 15 line 7 with the following amended paragraph:

It will be appreciated that the invention ~~utilises~~utilizes an amplifier having at its non-inverting input a first stack of bipolar transistors operating at first current density and provides in a feedback loop between the output of the amplifier and its inverting input, a second stack of bipolar transistors operating at second current density lower then that of the first stack. Due to the difference in current density of the two stacks, an enhanced ΔV_{be} is reflected at the output of the amplifier. This PTAT voltage is developed across a resistor coupled to the output of the amplifier and to a reference potential, typically ground. If this PTAT voltage is added to a balanced CTAT

voltage, a voltage reference insensitive to the temperature is provided. However, if the PTAT voltage is not superimposed or combined with a balanced CTAT voltage, then the voltage developed across the resistor is not temperature insensitive- the ΔV_{be} voltage is directly related to temperature fluctuations (see equation 1)- and as such the circuit may be used to provide a temperature sensor.

Please replace the paragraph beginning on page 15 line 21 with the following amended paragraph:

Figure 6 shows a simplified schematic of how such a circuit could be provided in accordance with the present invention to provide a voltage reference (i.e., insensitive to temperature fluctuations) and a temperature sensor (i.e., giving an output value related to the on-chip temperature). An amplifier is provided having an inverting and non-inverting input. At the output of the amplifier a resistor[[,]] r1[[,]] is provided[[:]], coupled between the output of the amplifier and ground. A first stack of diodes (D1, D2, D3) is provided and coupled to the non-inverting input of the amplifier. This first stack or chain is driven with a current[[,]] I3[[,]] which is desirably a PTAT current. A second chain of diodes is provided in a feedback loop between the inverting input and the output of the amplifier. This chain is driven with a second current[[,]] I6[[,]] and is adapted to operate at second current density lower then that of the first stack. It will be appreciated that equivalent[[ly]] bipolar transistors, suitably configured, could be used instead of the diodes mentioned and illustrated.

Please replace the paragraph beginning on page 16 line 3 with the following amended paragraph:

~~In use, if~~If the circuit is to be used as a temperature insensitive voltage reference, then it is important to remove any curvature components that are intrinsic to bandgap voltage circuits. It will be appreciated that a CTAT voltage provides a positive curvature contribution which can be ~~obviated~~countered by combining such a CTAT voltage with a negative curvature component of a

PTAT voltage.~~currents.~~ This may be created by providing the second current[[,]] I6[[,]] as a constant current source, such that when CTAT and PTAT voltages are added, the curvature component of each ~~cancelling~~cancels the other out.

Please replace the paragraph beginning on page 16 line 29 with the following amended paragraph:

It will be understood that examples of circuits implementing the present invention ~~has~~have been described with reference to a specific PNP configuration of bipolar transistors and that it is not intended that the application of the invention be limited to such configurations. As will be understood by the person skilled in the art, many modifications and variations in configurations may be achieved by implementation in NPN architectures or the like. Similarly, where transistors are provided in an nMOS or pMOS configuration, it will be appreciated that modifications can be made to change which transistors are provided in each configuration without departing from the spirit and scope of the invention. Furthermore, where the invention is described in a bipolar implementation, it will be appreciated that such an implementation can be provided using CMOS processes by using parasitic components and the like. It will be appreciated that what has been described herein is an exemplary embodiment of a bandgap voltage reference in accordance with the present invention. Specific components, features and values have been used to describe the circuit in detail but it is not intended that the present invention be limited in any way whatsoever except as may be deemed necessary in the light of the appended claims.